AMENDMENTS TO THE CLAIMS

1. (original) A drift compensation system comprising:

a first clock phase alignment circuit for providing an output clock signal which is frequency locked to an input reference clock signal,

a second clock phase alignment circuit having input thereto the output clock signal provided by said first clock phase alignment circuit,

first deviation means at an output of said first clock phase alignment circuit for providing a first deviation between a current clock phase of said first clock phase alignment circuit and an initial clock phase thereof;

second deviation means at an output of said second clock phase alignment circuit for providing a second deviation between a current clock phase of said second clock phase alignment circuit and an initial clock phase thereof; and

phase control logic for providing first phase shift signals as inputs to said first clock phase alignment circuit to cancel a phase shift between said output clock signal and said reference clock signal in response to a difference between said first deviation and said second deviation.

2. (currently amended) A drift compensation system according to claim 1, wherein

each of said first and second clock phase alignment circuits comprises a clock management circuit for providing said output clock signal which is frequency locked to said input reference clock signal, and

said phase control logic provides second phase shift signals in response to a comparison of said deviations~~said output clock signal~~, each of said second phase shift signals being an input step to said clock management circuit to reduce to zero said phase shift in a number of steps.

3. (original) A drift compensation system according to claim 2, wherein

said first deviation means and said second deviation means each include a register for storing an initial number of steps used at startup of the respective clock phase alignment circuit for reducing said phase shift to zero, and

a subtractor for subtracting said initial number of steps from a current number of steps necessary to reduce said phase shift to zero after said startup, in order to obtain respectively said first deviation or said second deviation.

4. (original) A drift compensation system according to claim 3, wherein each of said first phase shift signals provided by said phase control logic is input to said first clock phase alignment circuit to reduce to zero said phase shift between said output clock signal and said reference signal.

5. (original) A drift compensation method for canceling the phase drift in a drift compensation system including a first clock phase alignment circuit and a second clock phase alignment circuit, the first clock phase alignment circuit being adapted to provide an output clock signal frequency locked to an input reference clock signal, the method comprising the steps of:

aligning, at defined times, a clock phase in the second clock phase alignment circuit by frequency locking the output clock signal to the input reference signal;

determining a deviation for each of said first and second clock phase alignment circuits, where said deviation in a given circuit is characterized by a difference between a number of current steps needed for alignment of that circuit and a number of steps needed for the initial alignment;

checking whether the second deviation needed for said second clock phase alignment circuit is different from the first deviation needed for said first clock phase alignment circuit; and

if the second deviation is different from the first deviation, shifting by one step the phase of said first clock phase alignment circuit.

6. (original) A drift compensation method according to claim 5, wherein said step of shifting comprises shifting one step up if said second deviation is greater than said first deviation or shifting one step down if said second deviation is less than said first deviation.

7. (original) A drift compensation method according to claim 5, further comprising a step, before said aligning step, of aligning on startup said first clock phase alignment circuit and storing a number of phase shifts as an initial number of steps for said first clock phase alignment circuit.

8. (original) A drift compensation method according to claim 7, wherein the drift compensation system further includes phase control logic, and an aligned signal is provided by the first clock phase alignment circuit to the phase control logic when said circuit has been aligned.

9. (original) A drift compensation method according to claim 8, wherein said first clock phase alignment circuit provides a sampling clock when said circuit has been aligned, said sampling clock being used as a clock for data modules.

10. (original) A drift compensation method according to claim 9, wherein said second clock phase alignment circuit is enabled to be aligned when said aligned signal is provided by said first clock phase alignment circuit, the number of phase shifts needed for such an alignment being stored as an initial number of steps for said second clock phase alignment circuit.

11. (original) A drift compensation method according to claim 6, further comprising a step, before said aligning step, of aligning on startup said first clock phase alignment circuit and storing a number of phase shifts as an initial number of steps for said first clock phase alignment circuit.

12. (original) A drift compensation method according to claim 11, wherein the drift compensation system further includes phase control logic, and an aligned signal is provided by the first clock phase alignment circuit to the phase control logic when said circuit has been aligned.

13. (original) A drift compensation method according to claim 12, wherein said first clock phase alignment circuit provides a sampling clock when said circuit has been aligned, said sampling clock being used as a clock for data modules.

14. (original) A drift compensation method according to claim 13, wherein said second clock phase alignment circuit is enabled to be aligned when said aligned signal is provided by said first clock phase alignment circuit, the number of phase shifts needed for such an alignment being stored as an initial number of steps for said second clock phase alignment circuit.